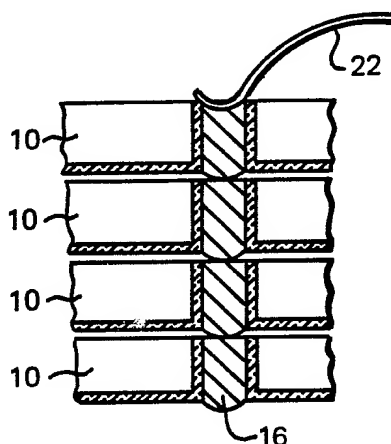




## INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

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**(54) Title:** STACKING OF INTEGRATED CIRCUITS**(57) Abstract**

An integrated circuit wafer (10) is made with a through-going plug (16) of electrically conductive material which protrudes above the wafer surface so that one can stack integrated circuits spaced from each other but interconnected electrically by the plugs (16) which extend therethrough in mutual contact.

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<sup>+</sup> Any designation of "SU" has effect in the Russian Federation. It is not yet known whether any such designation has effect in other States of the former Soviet Union.

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STACKING OF INTEGRATED CIRCUITS

5 This invention relates to the stacking of a plurality of integrated circuits on top of each other, and also to the product of that process and the intermediate product which forms part of the stack.

10 It is an object of the present invention to provide a method of stacking integrated circuits one on top of another in such a manner that they are electrically connected together and also in such a way that the resulting product can be processed and packaged in the normal manner using conventional assembly methods.

15 In accordance with the present invention there is provided an integrated circuit comprising a substrate having holes therethrough, said holes being filled with plugs of electrically conductive material which protrude above the surface of the substrate on at least one face of the substrate.

20 The invention also includes a stack of integrated circuits wherein the circuits are spaced from each other by the protruding plugs and are electrically interconnected by one or more such plugs of conductive material.

25 Also in accordance with the invention there is provided a method of fabricating a wafer for an integrated circuit which comprises the steps of making a hole through a wafer with an electrically insulating surface layer in the hole, and filling the hole with an electrically conductive material to form a plug which protrudes above the surface of the wafer on at least one face of the wafer.

30 Also in accordance with the present invention there is provided a method of fabricating a wafer for an integrated circuit, comprising the steps of making a

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5 well in the wafer with an electrically insulating surface layer, filling the well with a plug of electrically conductive material, grinding the wafer to remove the wafer material below the well thereby to expose the bottom of the electrically conductive material, and providing a protruding portion of electrically conductive material at at least one end of the plug.

10 In order that the invention may be more fully understood, one presently preferred embodiment will now be described by way of example and with reference to the accompanying drawings, in which:

15 Figs. 1 to 5 show the stages in the fabrication of the intermediate product of the invention; and

Fig. 6 shows a stack of individual integrated circuit chips.

20 As shown in Fig. 1, the first stage in the fabrication process of a silicon wafer 10 of initial thickness  $T$  is the creation of a plurality of deep wells 12 in the silicon wafer. These can be made by a suitable etching or cutting process. The wells 12 can be purpose-designed contact areas or existing bond pad sites, and the depth of the wells will depend upon the desired final wafer thickness.

25 As shown in Fig. 2, the internal surface of each well 12 is coated with a suitable insulating medium to form an insulating layer 14. If the wells are cut by a laser, with oxygen present, this will form a silicon oxide layer on the surface of the well, and in this case there will be no need for a separate insulating layer 14.

30 As shown in Fig. 3, the wells 12 are then filled with a suitable electrically conductive material 16, up to the top surface of the wafer, to form a plug.

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Next, the underside of the wafer 10 is ground away to reduce the wafer to a lesser thickness  $t$ . This exposes the conductive material 16 at the back surface of the wafer, as shown in Fig. 4.

5           Next, as shown in Fig. 5, the back of the wafer is covered by a suitable layer 18 of electrically insulating material and holes are made through this to the electrical contacts which are constituted by the plugs of electrically conductive material 16. After  
10 this, the back contact areas are covered by a "bump" of suitable electrically conductive material in order form a protruding pad 20. This pad 20 enables the fabricated wafer to become one component in a block or stack of wafers as shown in Fig. 6. With each pad 20  
15 contacting the top surface of the plug of the adjacent chip one has an electrical contact which extends through the plurality of chips and forms a continuous through contact. A suitable wire bond 22 can be connected to the through contact plug. The individual  
20 chips can be stacked together after wafer sawing, or a combination of different chips can be combined together.

Although in the embodiment described above the protruding pad is at the bottom of the wafer, one  
25 could alternatively or additionally provide a protruding pad at the upper face of the wafer.

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## CLAIMS:

5 1. An integrated circuit comprising a substrate having holes therethrough, said holes being filled with plugs of electrically conductive material which protrude above the surface of the substrate on at least one face of the substrate.

10 2. An integrated circuit as claimed in claim 1, in which the plugs protrude above a surface of the substrate which is otherwise covered with a layer of electrically insulating material.

15 3. An integrated circuit as claimed in claim 1 or 2, in which the holes have an electrically insulating surface layer.

20 4. A stack of integrated circuits as claimed in any preceding claim, wherein the circuits are spaced from each other by the protruding plugs and are electrically interconnected by one or more such plugs of conductive material.

25 5. A method of fabricating a wafer for an integrated circuit which comprises the steps of making a hole through a wafer with an electrically insulating surface layer in the hole, and filling the hole with an electrically conductive material to form a plug which protrudes above the surface of the wafer on at least one face of the wafer.

30 6. A method of fabricating a wafer for an integrated circuit, comprising the steps of making a well in the wafer with an electrically insulating surface layer, filling the well with a plug of electrically conductive material, grinding the wafer to remove the wafer material below the well thereby to expose the bottom of the electrically conductive material, and providing a protruding portion of  
35 electrically conductive material at at least one end of

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the plug.

7. A method as claimed in claim 6, which includes coating the wafer material around the exposed bottom of the plug with a layer of electrically  
5 insulating material.

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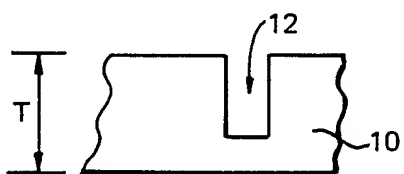
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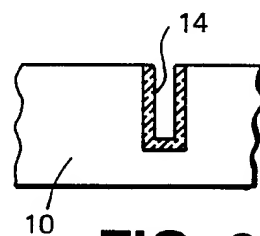
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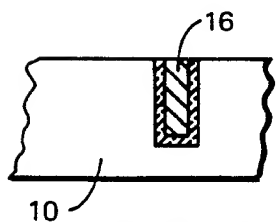
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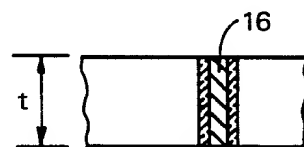
**FIG. 1**



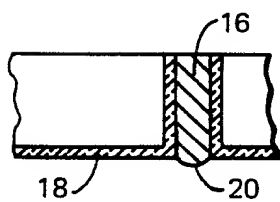
**FIG. 2**



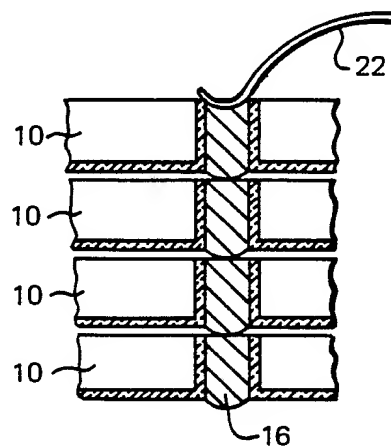
**FIG. 3**



**FIG. 4**



**FIG. 5**



**FIG. 6**